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Towards memristors supremacy with novel machine learning algorithms

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ABSTRACT

The von Neumann architecture for current computers is slowly showing signs of limitations, due to the finite bus rate between the RAM (memory) and the CPU (computing unit). In-Memory computing is an alternative to this architecture, which however is still in the early stages of development. Memristors are an analog and classical alternative, as these components can act both as a memory, or as a simple computing unit. When wired together, these can in fact be used for a variety of applications. During the course of our research, we have developed an in-depth experimental understanding of both the limitations and the real possibilities of these devices, and developed automated algorithms for their characterization; at the theoretical level, we have incorporated the experimental features to implement novel analog computing units for specific tasks. We have shown that memristors can tackle QUBO and cubic optimization problems, and exhibit tunneling phenomena.

TECHNICAL GOALS

The technical goals of this projects were concentrated around two pillars. The first was the development of a methodology to characterize and infer memristor parameters. This part was conducted by a team of both of engineers and physicists. The second was the development of machine learning algorithms both based on memristor behavior (characterized realistically), and machine learning algorithms able to automatically characterize memristors.

SCIENTIFIC APPROACH AND RESULTS

The main technical goals of the project have been essentially achieved. This goes beyond the academic standpoint of a good publishing record. For a start, we have efficient automatization algorithms able to infer automatically the parameters to characterize electronic memristors based on a combination of filamentary switching and tunneling junction. Moreover, we have been able to obtain a real model of memristor which fits the experimental results. In this part of the project, the designs of the experiments were mostly developed by Dale (co-Inv) and Caravelli (PI), and the development of the automated algorithm by Isaf (student). Most of the theory developed by the PI prior to this project was theoretical in nature and not completely grounded on realistic memristive behavior, but only focusing on algorithmics. However, part of the success of this project was in extending this theory to include a large class of memristor types. What we have shown in this project is that circuits of memristors are able to approximately solve QUBO problems similar to the Ising model, an NP-hard problem, and cubically constrained Hamiltonian. QUBOs are quadratically unconstrained binary optimization problems of the same class typically tackled by quantum computers such as D-Wave, while cubic problems are task specific and closer to the typical memristive behavior. Both problems can however be expressed as optimization tasks, and are thus of general practical interest.

We have tested our memristor-based algorithms against state of the art software, obtaining impressive results at a fraction of the effort (see Sheldon (postdoc), Caravelli, Coffrin (co-Inv) for instance). In addition, several automated algorithms for the analysis of the experimental data have been developed; this was led in particular by Lokhov (co-PI), Vuffray (co-Inv) and Coffrin.

Specifically, most of the algorithms based on ideal memristors for the solution of QUBO and cubic problems have been extended to realistic memristor models. We have in fact introduced a mapping between the exact optimization task and the circuit topology, which directly fits into the dynamics of memristive circuits. Moreover, Caravelli and Sheldon developed a new analytical technique to study these devices, which will be key for future analysis, and investigated the use of memristors for RC.

MISSION AGILITY

One of the science missions of the Laboratory is the development of novel computing architectures. Among these, one of the pillars is Beyond the von Neumann architecture, within the IS&T. This project naturally fits into this category. In particular, one of the latest findings, which occurred during the last year, is that circuits of memristor devices can in fact perform a tunneling phenomenon between energy barriers that is similar to the one typically seen in classical and thermal systems, or quantum and/or thermal nanoscale systems. Moreover, being memristors passive components, it also fits with the energy saving mission established by DOE. Algorithms implemented with memristors require in fact less battery than their CMOS counterpart implementation.

TECHNICAL VITALITY

The findings of our ER are novel, and not incremental. As far as we know, we were the first group investigating memristors and memristor-inspired algorithms that use these in the deep analog regime, in which all memristors are interacting, rather than used merely as memory in combination with FPGA board and/or CMOS. Also, we are essentially the only existing group worldwide able to theorize about the devices interactions, and offer a priori prediction. Aside from various publications and invitations to conferences of all the members of the group, the research of this ER was published in various high impact conferences such as NeurIPS, and high impact journals such as Science Advances.

WORKFORCE DEVELOPMENT

During the course of this work, we had initially 2 postdocs and 4 permanent members. One postdoc, F. C. Sheldon who received a CNLS fellowship, moved to away for a LIMS fellowship, while F. Caravelli is now a Staff member in T4. Aside from these two, the other co-Inv and the technical staff members were not exposed to memristor devices.

CONCLUSION

This grant not only has developed an important capability at the Lab, but has now an established Lab equipment and devices to continue the research in various venues. In particular, the novel algorithms developed in this grant will now be tested on harder grounds such as off-the-shelves machine learning. We will apply to further LDRD funding to further expand these developments.

ACRONYMS AND DEFINITIONS
QUBO – Quadratically unconstrained binary optimization
CMOS – Complementary metal-oxide semiconductor
ER – Exploratory Research
FPGA – Field programmable gate array
RC – Reservoir Computing

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